



AMIS-30660 - Power Dissipation in Case of Bus Failure

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APPLICATION NOTE

Introduction

The AMIS-30660 high speed CAN transceiver is designed to withstand bus failures. Without any damage to the IC the CANH or CANL line may be shorted to ground, V_{CC} or the battery supply. However in some bus failure conditions an increase in power dissipation might occur. This will lead to a rise in junction temperature.

Two bus states can be distinguished: recessive and dominant. In both states both CANH and CANL can be shorted to GND, V_{CC} or V_{BAT} . In this application note we are investigating the worst case conditions therefore short to V_{CC} is not discussed.

Recessive State

In the recessive state $TxD = 1$ and both CANH and CANL drivers are disabled. Figure 1 illustrates the equivalent schematic. R_{BUS} is the total impedance of the (split) termination on both end-sides of the CAN bus. The typical value is 60Ω . $R_{i,cm}$ is the common mode input impedance with a typical value of $25 \text{ k}\Omega$. V_{CC} is the 5 V supply. Without power ($V_{CC} = 0 \text{ V}$) the common mode voltage is still kept by a passive clamp but can be higher than $V_{CC}/2$. This particular condition is not taken into account in the calculations.

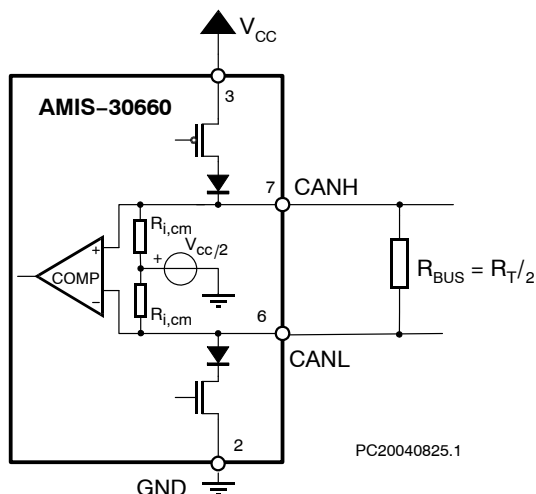


Figure 1. Equivalent Schematic in Recessive State

The power dissipation for the different bus-error conditions is given in Table 1.

Table 1. POWER DISSIPATION FOR CAN-BUS ERRORS IN RECESSIVE STATE

Bus	Short To	
	GND	V_{BAT}
CANL	$P \approx \frac{V_{CC}^2}{2R_{i,cm}}$	$P \approx \frac{2(V_{BAT} - V_{CC}/2)^2}{2R_{i,cm}}$
CANH	$P \approx \frac{V_{CC}^2}{2R_{i,cm}}$	$P \approx \frac{2(V_{BAT} - V_{CC}/2)^2}{2R_{i,cm}}$

Calculated for $V_{CC} = 5 \text{ V}$, $V_{BAT} = 24 \text{ V}$, $R_{i,cm} = 25 \text{ k}\Omega$ and $R_{BUS} \ll R_{i,cm}$ yields in:

Table 2. CALCULATED POWER DISSIPATION FOR CAN-BUS ERRORS IN RECESSIVE STATE

Bus	Short To	
	GND	V_{BAT}
CANL	0.5 mW	37 mW
CANH	0.5 mW	37 mW

Dominant State

In dominant state $TxD = 0$ and both drivers are active. In case of a short circuit the currents for both CANH and CANL are limited to $I_{O(sc)}$ which is 120 mA in worst case condition. Figure 2 illustrates the equivalent schematic.

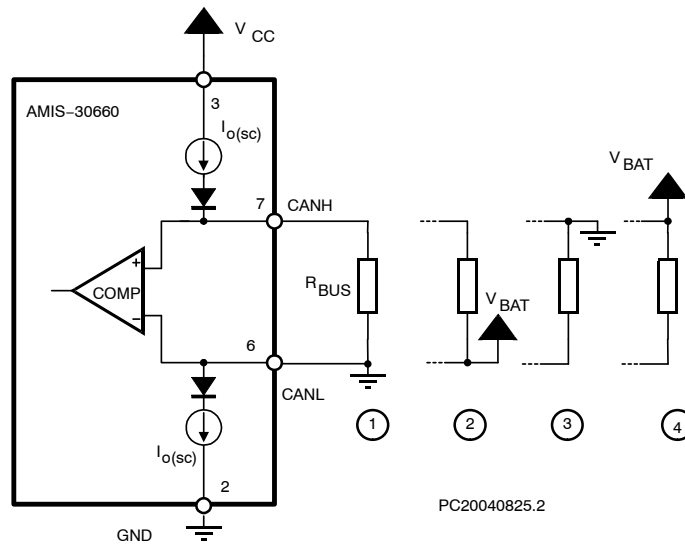


Figure 2. Equivalent Schematic in Dominant State

The power dissipation for the different bus-error conditions is given in Table 3.

Table 3. POWER DISSIPATION FOR CAN-BUS ERRORS IN DOMINANT STATE

Bus	Short To	
	GND	V _{BAT}
CANL	See Figure 2 Case (1) Bus Communication Possible but with Bit Timing Limitations	See Figure 2 Case (2) Both CANL/CANH are on V _{BAT} Level through R _{BUS} → No Communication Possible Time-Out by Master
	$P = \frac{(V_{CC} - V_{O(dom)CANH})^2}{R_{BUS}}$	$P = V_{BAT} \cdot I_{O(sc)}$
CANH	See Figure 2 Case (3) Both CANL/CANH are on GND Level through R _{BUS} → No Communication Possible Time-Out by Master	See Figure 2 Case (4) Bus Communication Possible but with Bit Timing Limitations
	$P = V_{CC} \cdot I_{O(sc)}$	$P = V_{BAT} \cdot I_{O(sc)} - R_{BUS} \cdot I_{O(sc)}^2$

Calculated for V_{CC} = 5 V, V_{BAT} = 24 V, R_{BUS} = 60 Ω, I_{O(SC)} = 120 mA and V_{O(dom)CANH} = 3.6 V yields in:

Table 4. CALCULATED POWER DISSIPATION FOR CAN-BUS ERRORS IN DOMINANT STATE

Bus	Short To	
	GND	V _{BAT}
CANL	108 mW	2.88 W (Note 1)
CANH	350 mW	2.02 W


1. Because no communication is possible, the master (depending on the application software) will cease the communication (= permanent recessive state) and the dissipated power drops to 37 mW.

Average Power Dissipation and Related Increase in Junction Temperature

The worst case condition from application point of view is a short to V_{BAT} on the CANH Pin in dominant state. Communication is still possible but the dissipation is 2.02 W giving the boundary conditions as stipulated in .

Calculating with a duty cycle of 50% (meaning 50% of the transmission time the bus is in dominant state) the average power dissipation is 1.01 W (neglecting the 37 mW dissipation in recessive state).

The thermal resistance of the package is 150 K/W in free-air. Soldered on a two layer PCB R_{th(vj-a)} < 100 K/W is expected. Calculating with 100 K/W yields in a worst case expected temperature increase of 101°C.

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